Akilesh Kannan

{Hard, Soft}ware tinkerer

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Education

INDIAN INSTITUTE OF TECHNOLOGY MADRAS
Jul 2018 - Jul 2023 | Chennai, India

Dual Degree (B.Tech & M.Tech) Electrical Engineering

CGPA: 9.17 / 10

- Ranked 592 (Top 0.23%) in JEE Advanced 2018 among over 250,000 candidates.
- Ranked 1319 (Top 0.13%) in JEE Main 2018 among 1 million candidates.

MAHARISHI VIDYA MANDIR
May 2018 | Chennai, India

Class XII, CBSE

Grade: 97.2%

- Awarded a KVPY SX Fellowship to pursue studies in basic sciences as a result of excellent performance in KVPY 2017.

Relevant Projects

GLOCAL TLB PREFETCHER Master's Project
Oct 2021 - May 2023

Prof. Madhu Mutyam

- Performed extensive literature reviews on existing works on TLBs, prefetchers and virtual memory.
- Worked on improving the performance of TLBs in multi-core systems by identifying memory access patterns across multiple cores.
- Devised a new prefetching mechanism targeting L1-TLBs that incorporated findings about repetitive memory access patterns in parallel applications, resulting in upto 50% TLB misses getting avoided in certain benchmarks.

OCTA-CORE NETWORK-ON-CHIP Undergraduate Intern
Oct 2020 – Apr 2021

RISE Lab, Dept. of CSE

- Worked on an Multi-Core Criticality-Aware Network-On-Chip enabled SoC implementing a Directory-Based Coherence Protocol for avionics applications.
- Helped porting the project to a Xilinx VCU-118 FPGA; identified and corrected multiple critical bugs that failed synthesis and implementation.
- Started the initiative of a design document to help understand the design architecture of the project for newcomers, and contributed >50%.

IN-MEMORY COMPUTE ENGINE Course Project
Jan 2022 - Jun 2022

Embedded Memory Design

- Thoroughly reviewed recent works in In-Memory Computation for Deep Learning.
- Performed extensive analyses to quantize the given floating-point model while minimising accuracy loss, being energy and layout area efficient.
- Implemented a SRAM-based charge-domain compute engine to perform Multiply Accumulate (MAC) operations; achieved 95.56% accuracy with approx. 400pJ/bit energy consumption for the trained model in hardware.

SINGLE CYCLE RISC-V PROCESSOR Hobby Project
May 2020 - Nov 2020

- Conceptualised and developed a fully parameterised RV32I processor in Verilog and synthesised for a Xilinx Arty A7-100T FPGA at 100MHz.
- Working on improving performance by pipelining the processor, with forwarding and stalling techniques.

Professional Experience

VENTANA MICROSYSTEMS Bangalore, India
Jul 2023 - Present

DV Engineer

- Worked on the design and verification of a RISC-V Vector Unit and Processor Cluster Interconnect Unit.
- Wrote and executed testplans for various phases of the design cycle from bringup to coverage closure.
- Developed multiple directed tests in assembly and random stimulus tests using UVM to identify potential bugs and corner cases.
- Analyzed coverage, generated and reviewed regression reports, developed scripts for automation.
- Identified as one of the top performers of the company and was given a SPOT award.

TEXAS INSTRUMENTS Bangalore, India
May 2022 - Jul 2022

Embedded Software Intern

- Worked with the automotive radar software team to develop a utility to upload the bootloader and applications over ethernet with low-level ethernet drivers.
- Reduced upload times from 5-10secs to <100msec using a reliability layer over UDP.
- Awarded a return offer to join full-time after graduation due to exceptional performance.

Areas of Interest

Core Computer Architecture, Processor Microarchitecture, Hardware Security, HW/SW co-design, HW Accelerators

Others Self-hosting, Reverse-engineering, Automation, Science communication, Open source Hardware

Skills

Programming C • C++ • Python • Shell • Lua • ASM (RISCV, x64) • SystemVerilog • Bluespec Systemverilog

Tools and Frameworks Vivado/Vitis HLS • gem5 • DynamoRIO • Linux • gdb • UVM • Docker • LaTeX • Questasim • Eldo • LTspice

Other Projects

CYCLE-ACCURATE PROCESSOR SIMULATOR, BRANCH PREDICTOR Course Project Jul 2021 - Nov 2021

Computer Architecture

- ➜ Created a cycle-accurate superscalar processor simulator in Python, with a custom ISA involving arithmetic and load store ops only; used Tomasulo's algorithm to model Out-of-Order execution capabilites.
- ➜ Implemented the Tournament Branch Predictor from Alpha21264 using the Branch Prediction Championship Kit from JILP 2016; adjudged best performing implementation in the class for the given storage constraints.

8-BIT MULTIPLIER Course Project Oct 2021 - Dec 2021

Digital IC Design

- ➜ Used GNU Electric to design and layout a transistor-level circuit of a signed 8-bit Multiplier, with ripple-carry adder and carry look-ahead adder for the vector merge stage.
- ➜ Used inverting full adders to optimize the area of the layout and pipelined the design, doubling the max clock frequency to 2.5GHz from 1.35GHz.

SYMPHONIES OF THE EM UNIVERSE Poster May 2020 - Nov 2020

Engineering Electromagnetics

- ➜ Explored the electromagnetics involved in Very Low Frequency emissions in the atmosphere due to lightning strikes, such as whistlers and hisses.
- ➜ Created and presented a poster on learnings to an audience of 200+ people during a poster day organised at the end of the course.

XV6: A TOY OS Lab Project Aug 2021 - Dec 2021

Operating Systems

- ➜ Worked on core concepts in OS, including process management, memory management, interrupt handling, file system, paging, scheduling, virtual memory, kernel and user-level interfaces.
- ➜ Upgraded the kernel to use Copy-On-Write (COW) memory management and lazy page allocation.

SPARSE MATRIX-VECTOR MULTIPLICATION ACCELERATOR Course Project Jan 2022 - Jun 2022

Mapping DSP Algorithms to Architectures

- ➜ Reviewed existing literature on accelerator designs for sparse matrix multiplication operations.
- ➜ Implemented a hybrid CPU/FPGA accelerator for sparse matrix vector multiplications.
- ➜ Reduced the number of multiplications to the bare minimum required, improving energy consumption and throughput.

Coursework

Graduate Computer Architecture • Secure Processor Microrchitecture • Embedded Memory Design • Mapping DSP Algorithms to Architectures • Digital Systems Testing • CAD for VLSI • Digital IC Design • Analog IC Design • RF IC Design

Undergraduate Operating Systems • Computer Organisation• Analog Circuits • Digital Signal Processing • Communication Systems

Teaching Assistantship

DIGITAL IC DESIGN Jul 2022 - Nov 2022

Prof. Janakiraman Viraraghavan

- ➜ Evaluated exams, assignments and course projects and held office hours for queries regarding assignments and course material.

APPLIED PROGRAMMING LAB Jan 2023 - May 2023

Prof. Nitin Chandrachoodan

- ➜ Evaluated programming assignments and held office hours to clarify students' questions.

Volunteering

AVANTI FELLOWS Aug 2018 - May 2019

Mentor

- ➜ Mentored class 11, 12 students for JEE, KVPY and other competitive exams.

OPEN SOURCE Aug 2022 - Present

Maintainer

- ➜ Maintainer for the GTKWave flatpak.